	Application No.	Applicant(s)
Notice of Allowability	10/643,691	KATO, KIYOSHI
Notice of Anomability	Examiner	Art Unit
	Tan T. Nguyen	2827
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT F of the Office or upon petition by the applicant. See 37 CFR 1.31	S (OR REMAINS) CLOSED in this a 5) or other appropriate communication RIGHTS. This application is subject	pplication. If not included on will be mailed in due course. THIS
1. $igspace$ This communication is responsive to <u>the amendment and</u>	the T.D filed on April 15, 2005.	
2. ☑ The allowed claim(s) is/are <u>1 and 91-181</u> .		
3. $igspace$ The drawings filed on <u>19 August 2003</u> are accepted by th	e Examiner.	
 4.		
Attachment(s)	r	
1. ☑ Notice of References Cited (PTO-892)		Patent Application (PTO-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)) 6. ☐ Interview Summar Paper No./Mail D	
 Information Disclosure Statements (PTO-1449 or PTO/SB. Paper No./Mail Date 	/08), 7. 🗌 Examiner's Amend	
4. Examiner's Comment Regarding Requirement for Deposit		nent of Reasons for Allowance
of Biological Material	9.	Jamour Z
		TAN T. NGUYEN PRIMARY FYAMINFR

U.S. Patent and Trademark Office PTOL-37 (Rev. 1-04) **GROUP 2800**

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The amendment and the Terminal Disclaimer submitted by Applicants on April
 2003 have been received and entered.

- 2. New claims 170-181 have been added.
- The following is an examiner's statement of reasons for allowance: /
 The closest prior art to the present invention is Bill et al. (U.S. Patent No.

5,754,475). Bill et al. disclosed a multiple-bits-per-cell flash EEPROM having a memory core array and a reference cell array. Bill et al. failed to show or suggest a combination of a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage and a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second voltage as claimed in claims 1 and 91-169. Bill et al. also failed to show or suggest the combination of a first and second reference voltage supply electrically connected to a first and second input terminal of a sense amplifier circuit, a write circuit electrically connected to a verify circuit, the memory transistor and the reference memory transistor as claimed in claims 170-181.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-

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1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen Primary Examiner Art Unit 2827 April 25, 2005